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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,477	06/25/2003	Rung-Nan Lu	B-5132 621035-2	5079

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EXAMINER	
TRAN, HENRY N	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,477	LU, RUNG-NAN	
	Examiner	Art Unit	
	Henry N. Tran	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Application has been examined. The original claims 1-24 are pending. The examination results are as follows.

Information Disclosure Statement

1. The examiner has considered the document listed in the Information Disclosure Statement (IDS) received 8/18/03 (see the attached form PTO-1449).

Specification

2. The disclosure is objected to because of the following informalities: An editorial error has been found on line 24 of page 7, wherein "I16ut signals" should be --input signals--.

Appropriate correction is required.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the: "first test transistors", "first input terminals", and "a reference voltage" (claim 1), "second test transistors", "second input terminals", and "second test signals" (claim 4), "display region", "a plurality of blocks", "a first block", "a first set of the input terminals", "a second block", "a second set of the input terminals" (claim 8), "sub pixel sections", "a first input terminal", and "a second input terminal" (claim 9), "first test transistors", "first test signals", "second test transistors", "second test signals", "first and second input terminals" (claim 16), "a plurality of input terminals" (claim 17) must be shown or the features canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002

do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-24 rejected under 35 U.S.C. 102(e) as being anticipated by Kodate et al. (U.S. Patent No. 6,784,862, hereinafter referred to as "Kodate").

5. Re claim 1, Kodate, Figs. 1 and 2, teaches an active matrix display device having a display region (7) consisting of sub-pixels (13) arrayed in a matrix fashion, the sub-pixels (13) having switching elements (14), comprising: a plurality of data and scan signal lines (11 and 12), and common voltage lines (11) (It's noted that the scan signal lines (11) are also considered as the common voltage lines) the for sending signals (a scan signal and a data signal) and a reference voltage (electrical signals) to the sub-pixels, see col. 4, lines 13-41; first test transistors (TFTs 22), each of which is connected to one of the plurality of scan signal lines (11) for sending first test signals provided by a plurality of first input terminals (31-35) (test terminals 31-35) thereto; and the plurality of first input terminals (31-35), each of which is connected to one of a plurality of the first test transistors (22); wherein each gate of the first test transistors (22) is connected to the first input terminal (35), and each of the common voltage lines (11) is connected to one of the input terminals (16), the first test transistors control inputs of the first test signals provided by the first input terminals (31-35) to the sub-pixels; see col. 5, lines 15-37.

6. Re claim 2, Kodate further teaches each of the sub-pixels (13) comprises: a switching transistor (14) having a gate coupled to one of the scan signal lines (11), a drain/source coupled to one of the data signal lines (12); and a storage capacitor (18) coupled between one of the

common voltage lines (11) and a source/drain of the switching transistor (14), see Fig. 2, and col. 4, lines 22-38.

7. Re claim 3, Official Notice is taken for the claim elements: "a data driver generating the data signals" and "a scan driver generating the scan signals" because they are required elements in an active matrix display device (see Kim et al. Patent US 6,839,121; col. 1, lines 47-61).

8. Re claim 4, Kodate further teaches the use of second test transistors (22), each of which is connected to one of the plurality of the data signal lines (12) for sending second test signals thereto; and a plurality of second input terminals 16 and 51-53 (test terminals 16 and 41-53), each of the second input terminals is connected to one of a plurality of the second test transistors; wherein each gate of the second test transistors is connected to the second test terminal (53), and each of the common voltage lines (It's noted that the data signal lines 12 are considered as the common voltage lines) is connected to one of the second input terminals (16), the second test transistors control inputs of the second test signals to the sub-pixels.

9. Re claims 5-7, which comprise similar claim limitations of claims 1-3, rephrased to include a facing substrate having a common electrode, and a liquid crystal sealed between the array and facing substrate. Kodate also teaches include a facing substrate having a common electrode (a common electrode on the opposing substrate 3), and a liquid crystal sealed between the array and facing substrate, see col. 3, line 65 to col. 4, line 13). Claim 5-7 are therefore rejected on the same reasons set forth in claims 1-3, and the reasons noted above.

10. Re claim 8, which comprise the claim limitation of claim 1, rephrased to claim the display region is composed of a plurality of blocks, the scan signal lines included in a first block

of the plurality of blocks are connected to a first set of the input terminals via sources/drains of the test transistors, and the scan signal lines included in a second block of the plurality of blocks are connected to a second set of the input terminals different from the first set of the input terminals via the sources/drains of the test transistors. Kodate clearly teaches the display region (7) is composed of a plurality of blocks, e.g., display areas 61 and 62, the scan signal lines included in a first block (61) of the plurality of blocks are connected to a first set of the input terminals (16, 31 and 32) via sources/drains of the test transistors (22), and the scan signal lines included in a second block (62) of the plurality of blocks are connected to a second set of the input terminals (16, 33 and 34) different from the first set of the input terminals via the sources/drains of the test transistors; see Fig. 2, and col. 5, lines 38-54.

11. Re claim 9, Kodate teaches Figs. 1 and 2, teaches an active matrix display device comprising: an array substrate (2) having sub pixel sections (13) arrayed in a matrix fashion, each sub pixel section (13) having switching element (14), comprising: a plurality of data signal lines (12) and a plurality of scan signal lines (11) for sending data and scan signals to the sub pixel sections 13, see col. 4, lines 13-41; test transistors (TFTs 22), each of which is connected to one of the plurality of scan signal lines (11) for sending test signals provided by a plurality of input terminals (16 and 31-35) (test terminals 31-35) thereto; and the plurality of input terminals (16 and 31-35) for inputting test signals; wherein drains or sources of the test transistors (22) are connected to the scan signal lines (11), gates of a plurality of the test transistors (22) and the common voltage lines (11) (It's noted that the scan signal lines (11) are also considered as the common voltage lines) are connected to a first input terminal (16 and 35) of the plurality of input

terminals, the sources or drains of a plurality of the test transistors (22) are connected to a second input terminal (31-34) of the plurality of input terminals, and the test transistors control inputting of the test signals to the sub pixel sections, see Fig. 2, and col. 5, lines 22-41.

12. Re claim 10, Kodate further teaches switching elements (14) of the sub pixel sections (13) and the test transistors (22) are thin film transistors formed of amorphous silicon, see col. 2, lines 59-65.

13. Re claim 11, Kodate further teaches the sources or drains of the test transistors (22) that are connected to adjacent ones of the data signal lines (12) are connected to different ones of the plurality of input terminals, e.g., terminals 41, 42, 45 and 46; see Fig. 2.

14. Re claim 12, Kodate further teaches the sources or drains (23) of the test transistors (22) that are connected to adjacent ones of the scan signal lines (11) are connected to different ones of the plurality of input terminals (31, 32, 33 and 34), see Fig. 2.

15. Re claim 13, Kodate further teaches the gates (25) of all of the test transistors (22) connected to the scan signal lines (11) on the array substrate (2) are connected to the first input terminal (35).

16. Re claim 14, Official Notice is taken for the claim elements: "a drive circuit connected to ..., all of the test transistor are held in an OFF state" because the drive circuit which inputs the screen signals to the sub pixels (13) for displaying desired images are required features in an active matrix display device when testing is not needed or has been done.

17. Re claim 15, Kodate further teaches an opposing substrate (3) opposite to the array substrate (2), see Fig. 1, and col. 3, lines 49-62.

By the above reasons, claims 9-15 are rejected.

18. Re claim 16-24, which are method and apparatus claims that comprise similar claim elements and limitations recited in claims 1-15, and are therefore rejected on the same reasons discussed above.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. They are U.S. Patents Nos.: 6,924,875 to Tomita, 6,853,364 to Kai et al, 6,100,865 to Sasaki, 6,624,857 to Nagata et al., and 6,839,121 to Kim et al. that teaches methods and apparatuses for inspecting or testing active matrix display devices.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry N. Tran whose telephone number is 571-272-7760. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick N. Edouard can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Henry N. Tran

Henry N Tran
Primary Examiner
Art Unit 2674

HT
12/1/05